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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,587	10/03/2003	Wei-Hung Huang	JCLA5547-CA	2486

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/678,587	HUANG, WEI-HUNG
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 October 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-9</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-9</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>03 October 2003</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☒ Certified copies of the priority documents have been received in Application No. <u>09/491,201</u>.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Drawings

1.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5)

because they do not include the following reference character(s) mentioned in the

description: '116' in line 8 of page 2. Corrected drawing sheets are required in reply to

the Office action to avoid abandonment of the application. Any amended replacement

drawing sheet should include all of the figures appearing on the immediate prior version

of the sheet, even if only one figure is being amended. The replacement sheet(s)

should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so

as not to obstruct any portion of the drawing figures. If the changes are not accepted by

the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in

abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they

include the following reference character(s) not mentioned in the description: '112', '114,

and '126' in Figure 1. Corrected drawing sheets, or amendment to the specification to

add the reference character(s) in the description, are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the

sheet, even if only one figure is being amended. The replacement sheet(s) should be

labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2.   The abstract of the disclosure is objected to because it appears to be a foreign translation replete with grammatical errors and is not written in correct Idiomatic English. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

3.   Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Shimoda; Kenji et al. (US 5404248 A, hereafter referred to as Shimoda) in view of

Lahmeyer; Charles R. (US 4649541 A.)

35 U.S.C. 103(a) rejection of claims 1 and 7.

Shimoda teaches an apparatus for accessing data stored on an optical disc (See col. 2,

lines 32-44 in Shimoda), comprising: a row data interface, for receiving a demodulated

row data from the optical disc (demodulation/TBC circuit 207 in Figure 3 of Shimoda is a

row data interface, for receiving a demodulated row data from the optical disc; Note:

Figures 8A-8C in Shimoda teach that columns are Q encoded and then rows are P

encoded, hence data stored on the CD is row data); a first buffer, for storing the row

data from the row data interface (Memory 251 in Figure 9B in Shimoda is a first buffer,

for storing the row data from the row data interface); a first decoder, for performing a

first decoding to the row data stored in the first buffer and generating decoded data (P-

Series Row Decoding Circuit 252 in Figure 9B of Shimoda is a first decoder, for

performing a first decoding to the row data stored in the first buffer and generating

decoded data), wherein the decoded data is stored into a memory (decoded data from

P-Series Row Decoding Circuit 252 in Figure 9B of Shimoda is stored into Memory

257), the decoded data is also sent to an error detection code generator (decoded data

from P-Series Row Decoding Circuit 252 in Figure 9B of Shimoda is also sent to an

error detection code generator R-Series Decoding Circuit 254), the error detection code

generator R generates the error detection codes for the decoded data, the generated

error detection codes are stored into the memory (the error detection code generator -

Series Decoding Circuit 254 in Figure 9B of Shimoda generates the error detection

codes for the decoded data from P-Series Row Decoding Circuit 252, the generated

error detection codes are stored into the Memory 257); and a second decoder, for

reading the error detection codes from the memory (Q-Series Row Decoding Circuit 258

in Figure 9B of Shimoda is a second decoder, for reading the error detection codes from

the Memory 257), and performing a second decoding on the data stored in the memory

when the data stored in the memory is sufficient to be assembled as a complete data

block (Q-Series Row Decoding Circuit 258 in Figure 9B of Shimoda is a second decoder

for performing a second decoding on the data stored in the memory when the data

stored in the memory is sufficient to be assembled as a complete data block).

However Shimoda does not explicitly teach the specific use of storing the error

detection codes into a second buffer other than the memory.

Lahmeyer, in an analogous art, teaches that the Reed-Solomon Decoder of Figure 1 in

Lahmeyer has its own RMM Buffer 30. Note: col. 4, lines 1-5 in Shimoda teach that the

decoders in Shimoda are Reed-Solomon decoders, i.e., Q-Series Row Decoding Circuit

258 in Figure 9B of Shimoda is a Reed-Solomon decoder, but does not teach the

internal circuitry of the Reed-Solomon decoder. On the other hand, Lahmeyer teaches

the internal circuitry for a Reed-Solomon decoder required by the Shimoda patent to

make the circuitry in the Shimoda patent operational.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Shimoda with the teachings of Lahmeyer by including use

of internal circuitry for a Reed-Solomon decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of internal circuitry for a Reed-Solomon decoder would have provided the opportunity to make the circuitry in the Shimoda patent operational.

35 U.S.C. 103(a) rejection of claim 2.

See Error Computation and Correction Module 48 in Figure 1 of Lahmeyer.

35 U.S.C. 103(a) rejection of claims 3-6, 8 and 9.

Shimoda and Lahmeyer substantially teach the claimed invention described in claims 1 and 2 (as rejected above).

However Shimoda and Lahmeyer do not explicitly teach the specific use of embedded memory.

The Examiner asserts that it would be obvious to create a specific embodiment of the teachings in the Shimoda and Lahmeyer patent using a specific type of memory based on obvious engineering design requirements such as available space, hardware requirements and speed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Shimoda and Lahmeyer by including use of embedded memory. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the

art would have recognized that use of embedded memory would have provided the

opportunity to create a specific embodiment of the teachings in the Shimoda and

Lahmeyer patent using a specific type of memory based on obvious engineering design

requirements such as available space, hardware requirements and speed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4.   Claims 1-9 are rejected under the judicially created doctrine of obviousness-type

double patenting as being unpatentable over claims 5-10 of U.S. Patent No. US

6662335 B1 in view of Roth; Ron M. et al. (US 5719884 A, hereafter referred to as

Roth).

Double patenting rejection of claims 1-9.

Claims 5-10 of U.S. Patent No. US 6662335 B1 teach An apparatus for accessing data stored on an optical disc, comprising: a row data interface, for receiving row data which is EFM-demodulated (Eight-to-Fourteen-Modulation-demodulated) from the data accessed from the optical disc; a first buffer, for storing the row data from the row data interface; a first inner-code decoder, for performing inner-code parity decoding to the row data stored in the first buffer and generating inner-code decoded data, the inner-code decoded data is stored into a memory, the inner-code decoded data is also sent to an error detection code generator from the first inner-code decoder if the inner-code decoded data is required for generating an error detection code, the error detection code generator generates the error detection codes for the inner-code decoded data sent from the inner-code decoder, the generated error detection codes are stored into the memory; and an RSPC (Reed Solomon Product Code) decoder, for reading the error detection codes from the memory, storing the error detection codes into a second buffer other than the memory, and performing outer-code parity decoding on the data stored in the memory when the data stored in the memory is sufficient to be assembled as a complete data block.

However claims 5-10 of U.S. Patent No. US 6662335 B1 do not explicitly teach the specific use of a row decoder.

Roth, in an analogous art, teaches a row decoder.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claims 5-10 of U.S. Patent No. US 6662335 B with the teachings of Roth by including use of a row decoder. This modification would have
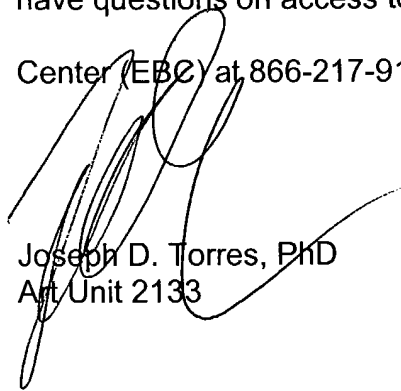
been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a row decoder would have provided the opportunity to decode row encoded data.

Conclusion

5.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133